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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,983	11/18/2003	Masanori Owaki	XA-9992	3658

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MCLEAN, VA 22102-3833

EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/714,983	OWAKI ET AL.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/18/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/714983 Attorney's Docket #: XA-9992
Filing Date: 11/18/2003; claimed foreign priority to 11/28/2002

Applicant: Owaki et al.

Examiner: Alexander Williams

Applicant's election of the species of figures 1-9 (claims 1 to 5), filed 4/18/06, has been acknowledged.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claims 1 to 5 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, it is unclear and confusing to what is meant by "**bonding wires** connected the bonding pads of said second semiconductor chip and corresponding electrodes formed on said mounting board; and a sealing member for encapsulating said plurality of first semiconductor chips, said second semiconductor chip and **the said**

bonding wire on said mounting board." In the claim, are there one bonding wire or a plurality of bonding wires on said mounting board?

In claim 3, it is unclear and confusing to what is meant by "being interconnected through said bonding wire." Is there only one bonding wire or a plurality of bonding wires connected here?

In claim 3, it is unclear and confusing to what is meant by "wherein said microcomputer and *said random access memory or said signal processing device* for processing the signal for specified application which is connected to said microcomputer are interconnected by wiring formed on the mounting board by imposition; and wherein said microcomputer includes an exclusive interface corresponding to **said nonvolatile memory**, *said microcomputer and said nonvolatile memory* being interconnected through said bonding wire." The use of "or" and "and" appear to be improper, unclear and confusing to what or if what is claimed.

In claim 5, it is unclear and confusing to what is meant by the claimed elements depending from previously claim structure.

Any of claims 1 to 5 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 to 5, **insofar as they can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Suzuki et al. (U.S. Patent # 6,815,746 B2).
1. Suzuki et al. (figures 1 to 37(b)) specifically figure 5 show a multi-chip module **1** comprising: a plurality of first semiconductor chips **5,6** surface-mounted on a surface of a mounting board **2** for exchanging signals with each other; a second semiconductor chip **(6 stacked on 5)** mounted back-to-back with at least one of said plurality of first semiconductor chips, said second semiconductor chip having most of bonding pads (inherent) thereof arranged along one side thereof; bonding wires **9** for connecting the bond pads of said second semiconductor chip and corresponding electrodes **7p** formed on said mounting board; and a sealing member **3** for encapsulating said plurality of first semiconductor chips, said second semiconductor chip and said bond wire on said mounting board.

2. A multi-chip module according to claim 1, Suzuki et al. show wherein said plurality of first semiconductor chips include a microcomputer, a RAM and a signal processing device for processing signals for specific applications, respectively and wherein said second semiconductor chip is a nonvolatile memory.

3. A multi-chip module according to claim 2, Suzuki et al. show wherein said microcomputer and said RAM or said signal processing device for processing the signal for specified application which is connected to said microcomputer are interconnected by wiring formed on the mounting board by imposition; and wherein said microcomputer includes an exclusive interface corresponding to said nonvolatile memory, said microcomputer and said nonvolatile memory being interconnected through said bonding wire.

4. A multi-chip module according to claim 3, Suzuki et al. show wherein said nonvolatile memory is mounted back-to-back with said first semiconductor chips including said microcomputer.

5. A multi-chip module according to claim 4, Suzuki et al. show wherein said first semiconductor chips mounted back-to-back with said nonvolatile memory include said microcomputer and said RAM; and wherein the long side of the semiconductor chip constituting said RAM and the long side of the semiconductor chip constituting said nonvolatile memory are arranged orthogonally to each other.

(7) Various semiconductor devices (ICs) have been built in the personal digital assistant (PDA). For example, a central processing unit (CPU), an application specific integrated circuit (ASIC), a synchronous dynamic random access memory (SDRAM: Synchronous Dynamic Random Access Memory) used as a memory, a flash memory, etc. are mounted on a printed circuit board (wiring board). Most of them are respectively mounted on the printed circuit board as single items. Therefore, the whole packaging area of these semiconductor devices increases and hence this interferes with the scale down of the electronic device such as PDA or the like. Each individual packaging of the semiconductor devices in the electronic device will produce a suspicion that the length of each of wirings for connecting between external electrode terminals of each semiconductor device becomes long, and bring about a possibility that a reduction in signal transfer speed and the like will occur.

(8) On the other hand, an example (MCP: Multi Chip Package) in which a static memory (SRAM: Static Random Access Memory) and a flash memory (flash nonvolatile memory) used as memories are built in a single package, has been commercialized by various manufacturers. However, the example with the SDRAM and the flash memory integrated into one has not heretofore been attained. A main application for the MCP commercialized up to now is a memory for a cellular phone. This is because the SRAM low in power consumption as compared with the SDRAM is used in the cellular phone. However, since the PDS needs a memory having larger capacity, the SDRAM other than the SRAM is used.

(9) An object of the present invention is to provide a small-sized and inexpensive semiconductor device wherein a dynamic random access memory such as a synchronous dynamic random access memory and a flash memory are built in a single encapsulater.

(5) The semiconductor device (system memory module) 1 according to the present embodiment 1 has such a structure as shown in FIGS. 1 through 7. FIG. 1 is a plan view of the semiconductor device in which an encapsulater is partly cut away, FIG. 2 is a plan view of the semiconductor device, FIG. 3 is a side view of the semiconductor device, and FIG. 4 is a bottom view of the semiconductor device, respectively.

(6) In the present embodiment 1, an example in which one flash memory chip and two dynamic random access memory chips are built in a single encapsulater, will be explained as a system memory module. The flash memory chip is a semiconductor chip with a 32-Mbit flash memory built therein, whereas each of the dynamic random access memory chips is a synchronous dynamic random access memory chip with a 64-Mbit synchronous dynamic random access memory built therein. FIG. 1 is a typical diagram showing the state of layout of the three semiconductor chips, and conductive wires for connecting electrodes of these semiconductor chips and electrodes of a wiring board.

(7) As shown in FIGS. 1 through 4, the semiconductor device (system memory module) 1 has, in appearance, a square and plate-shaped wiring board 2 (see FIGS. 1, 3 and 4), an encapsulater (package) 3 having the same outer dimensions as the wiring board 2, which is superimposed on a main surface (upper surface in FIG. 3) of the wiring board 2, and a plurality of protruded electrodes (bump electrodes) 4 provided on the back surface

(lower surface in FIG. 3) corresponding to a surface opposite to the main surface of the wiring board 2. The bump electrodes 4 are arranged in line (in an array form).

(8) In the present embodiment 1, the bump electrodes 4 are provided in the form of a frame-shaped array configuration wherein they are aligned in three rows along the longitudinal and transverse sides of the square wiring board 2. The numbers of the outermost-peripheral bump electrodes 4 arranged along the respective sides result in 15 respectively. The number (number of pins) of the whole bump electrodes 4 reaches 144 pins. The package 3 is made up of an insulating resin having a constant thickness and its peripheral surface is formed by cutting a block encapsulater formed by block encapsulation by dicing upon manufacture. Therefore, the peripheral surface results in a surface cut by dicing. When the block encapsulater is cut by a blade having a constant thickness although the peripheral surface of the package 3 varies according to the shape of a blade at dicing, its cut surface, i.e., the peripheral surface of the package 3 results in a surface normal to the main surface of the wiring board 2 as shown in FIG. 3.

(9) In the system memory module 1 according to the present embodiment 1, a flash memory chip 5 and a synchronous dynamic random access memory chip (SDRAM chip) 6 both shaped in the form of a rectangle, are respectively fixed to the main surface of the wiring board 2 side by side in parallel in a state in which a plurality of electrodes 7f and 7d on the surfaces thereof are being exposed and in such a manner that their long sides are provided face to face with each other. Another SDRAM chip 6 is fixed onto the flash memory chip 5. The system memory module 1 can be reduced in size owing to such lamination fixing.

(10) The flash memory chip 5 has a structure wherein a plurality of electrodes 7f are arranged in a row along the edge of each short side thereof. The long side of the flash memory chip 5 is longer than the long side of the SDRAM chip 6. When the SDRAM chip 6 is fixed onto the flash memory chip 5, the electrodes 7f provided along both short sides of the flash memory chip 5 can be exposed out of the SDRAM chip 6.

(11) Thus, the respective electrodes 7f arranged along both short sides of the flash memory chip 5, and the electrodes 7p provided on the main surface of the wiring board 2 can be connected to one another by conductive wires 9.

(12) The SDRAM chip 6 fixed to the main surface of the wiring board 2 and the SDRAM chip 6 fixed onto the flash memory chip 5 are identical in size and structure. Further, the electrodes 7d provided on the SDRAM chips 6 are disposed side by side along their long sides. Namely, the electrodes 7d of the SDRAM chip 6 are provided so as to take such a center-line layout configuration that they are arranged in a row from the center of one short side of the SDRAM chip 6 to the center of the other short side thereof. The electrodes 7p are provided on the main surface of the wiring board 2 on both sides of fixed areas of the SDRAM chips 6 so as to extend along the edges of the SDRAM chips 6.

(13) One ends of the wires 9 are respectively connected to the electrodes 7d having the center-line layout configuration. These wires 9 are divided from side to side, and the other one ends thereof are respectively connected to the electrodes 7p on the main surface of the wiring board 2, which are disposed on both sides of each SDRAM chip 6. While wire-connecting electrodes 7p lying between the SDRAM chip 6 and the flash memory chip 5 are shown in two rows in FIG. 1, the leading ends of the wires 9 extending from the electrodes 7d of the right-and-left SDRAM chips 6 are actually connected to both ends of slender electrodes 7p (see FIG. 5). Assuming that portions connected to the electrodes of each semiconductor chip are represented as first bonding points upon wire bonding, portions connected to the electrodes on the wiring board are represented as second bonding points. In FIG. 1, the electrodes 7p on the wiring board 2 indicate the second bonding points respectively.

(14) The system memory module 1 according to the present embodiment 1 has a structure wherein the 32-Mbit flash memory chip 5 and the two 64-Mbit SDRAM chips 6 are built in the single package 3, and has outer dimensions which are 13 mm long, 13 mm wide and 1.5 mm in height. As the bump electrodes 4, solder balls each having a diameter of 0.35 mm are used. The length of each bump electrode 4 that protrudes from the wring board 2, results in about 0.25 mm. Further, the pitch of each bump electrode 4 becomes 0.8 mm.

(15) Cross sections of a specific system memory module 1 are shown using FIGS. 5 and 6. FIG. 5 is an enlarged cross-sectional view taken along line A--A of FIG. 1, and FIG. 6 is an

enlarged cross-sectional view taken along line B--B of FIG. 1, respectively.

(16) As shown in FIGS. 5 and 6, a wiring board 2 comprises a multilayer structure wherein wirings 7 each shaped in a predetermined pattern are provided on a main surface and a back surface of a wiring board 1 and in one or more middle layers, and upper and lower wirings 7 are electrically connected to one another by conductors 7a (wirings) charged into through holes. The wring board 2 serves as a 4-layer BT (bismaleimide triazine) substrate having a thickness of about 0.2 mm, for example. The wirings 7 constitute electrodes 7p for connecting wires 9 on the main surface of the wiring board 1, and electrodes 7c used as bases for fixing bump electrodes 4 are provided on the back surface of the wiring board 1.

(17) Since the two semiconductor chips are mounted on the main surface of the wiring board 2 as already described above, the electrodes 7p for connecting the wires are disposed around chip mounting areas for mounting these semiconductor chips.

(18) Insulating films (solder resists) 10 and 11 are respectively formed on the main surface (upper surface) and back surface of the wiring board 2 as predetermined patterns so as to cover the wirings and the like. The electrodes 7p on the main surface of the wiring board have such structures that they are exposed so as to be capable of wire bonding, whereas the electrodes 7c on the back surface of the wiring board have such structures that they are exposed to fix the bump electrodes 4. Therefore, the insulating films 10 and 11 on the main surface side of the wiring board 2 have such structures that constant widths are cut away to define open grooves 12 and the electrodes 7p are exposed at the bottoms of the open grooves 12 (see FIG. 1).

(19) The two second bonding points are exposed within an open groove 12a defined in the main surface of the wiring board 2 between the right and left SDRAM chips 6 so that the other ends of the wires 9 whose one ends are connected to their corresponding electrodes 7d of the SDRAM chips 6 as viewed on the right and left sides of the open groove 12a, are both connected thereto. Namely, the second bonding points for wire bonding are arranged within the open groove 12a in two rows along its extending direction. As to the second bonding

points, both ends of the single long electrodes 7p are actually used as the second bonding points.

(20) As shown in FIGS. 5 and 6, a flash memory chip 5 and a SDRAM chip 6 shaped in a rectangular form are respectively fixed onto the insulating film 10 on the main surface of the wiring board 2 with adhesives 13 interposed therebetween, in parallel such that their long sides are opposite to one another. Further, a SDRAM chip 6 is fixed onto the flash memory chip 5 with an adhesive 14 similar to the above interposed therebetween. The SDRAM chip 6 directly fixed to the wiring board 2, and the laminated SDRAM chip 6 fixed onto the flash memory chip 5 are both SDRAMs identical in size and function. They are 64-Mbit SDRAMs, for example. The adhesives 13 and 14 make use of non-conductive paste, e.g., insulating epoxy resin paste. After they have been adhered to one another, the adhesives 13 and 14 are subjected to hardening (baking) at a temperature of about 150.degree. C., for example to reliably fix the semiconductor chips.

(21) Both the flash memory chip 5 and the SDRAM chip 6 become rectangular. The width of the SDRAM chip 6, i.e., the short side thereof is slightly shorter than the width (short side) of the flash memory chip 5. Further, the long side of the flash memory chip 5 becomes longer than the long side of the SDRAM chip 6. When the center of the SDRAM chip 6 is superposed on the center of the flash memory chip 5 so as to coincide with each other, short-side portions at both ends of the flash memory chip 5 are located away from the SDRAM chip 6, and electrodes 7f provided at the short sides thereof are exposed to such an extent that they are capable of wire bonding sufficiently.

(22) Thus, as shown in FIGS. 1 and 6, the SDRAM chip 6 is fixed onto the flash memory chip 5 with the adhesive 14 interposed therebetween in such a manner that the wiring bonding is made possible and the electrodes 7f on the sides of both short sides of the flash memory chip 5 are exposed. The electrodes of the SDRAM chip 6 are disposed in a row along its longitudinal direction and its center (center-line layout configuration: see FIG. 1).

(23) A description will now be made of the reason why the electrodes 7f are arranged along the short sides of the flash memory chip 5 in the flash memory chip 5. As different from an

SDRAM, a flash memory needs not to take into consideration a high-speed operation. Therefore, electrodes (pads) can be provided around a semiconductor chip to make in-chip wring lengths long and shorten wire lengths at wire bonding. When the semiconductor chip is rectangular in the case of the peripheral pads and the number of the pads is low, the pads can be provided at either long sides (long-side pads) or short sides (short-side pads).

(24) When the pads are adopted as the long-side pads, the routing of wirings on the wiring board becomes very complex as compared with the case where the pads are adopted as the short-side pads. Therefore, the short-side pads are apt to be used although there are other reasons. Even in the present embodiment 1, the flash memory chip is adopted in which the short-side pads are arranged.

(25) On the other hand, the respective electrodes 7f and 7d of the flash memory chip 5 and SDRAM chip 6 fixed to the wiring board 2 in parallel and the SDRAM chip 6 fixed onto the flash memory chip 5, and the electrodes on the wiring board 2 are respectively connected to one another by conductive wires, e.g., gold wires. Namely, the electrodes 7f and 7d of the flash memory chip 5 and two SDRAM chips 6, and the electrodes 7p of the wiring board 2 are connected to one another by their corresponding conductive wires 9 (see FIGS. 1, 5 and 6).

(26) These three semiconductor chips and wires 9 or the like are covered with an encapsulater (package) 3 formed over the whole main surface of the wiring board. The package 3 is formed of an insulting resin. In a method of manufacturing the semiconductor device according to the present embodiment 1, three semiconductor chips are respectively mounted on respective product forming areas of a sheet of large wiring board. Thereafter, a block encapsulater or package made up of an insulating resin is formed to a constant thickness on the main surface side of the wiring board by a transfer molding device. Finally, the wiring board and the block encapsulater are formed by dicing at the boundaries of the respective product forming areas. Therefore, the side faces of the package 3 result in surfaces cut by dicing and result in surfaces normal to the main surface of the wiring board 2.

(27) On the other hand, a plurality of protruded electrodes (bump electrodes) 4 are formed on the back surface (lower

surface in FIGS. 5 and 6) corresponding to a surface opposite to the main surface of the wiring board 2. The bump electrodes 4 are solder bump electrodes formed of solder balls formed so as to be superposed on their corresponding electrodes 7c. As the solder balls, solder balls each having a diameter of 0.35 mm, for example are used, and the bump electrodes 4 protrude from the back surface of the wiring board 2 by about 0.25 mm. The bump electrodes 4 are provided in the form of a frame-shaped array configuration as described above.

Claims 1 to 5, **insofar as they can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Taguchi (U.S. Patent Application Publication # 2002/0066956 A1).

1. Taguchi (figures 1 to 8) specifically figures 1A-C, 3A-C and 8 show a multi-chip module **1** comprising: a plurality of first semiconductor chips **5** surface-mounted on a surface of a mounting board **3** for exchanging signals with each other; a second semiconductor chip **7** mounted back-to-back with at least one of said plurality of first semiconductor chips, said second semiconductor chip having most of bonding pads (inherent) thereof arranged along one side thereof; bonding wires **9** for connecting the bond pads of said second semiconductor chip and corresponding electrodes formed on said mounting board; and a sealing member **(shown in figure 1B, but not labeled)** for encapsulating said plurality of first semiconductor chips, said second semiconductor chip and said bond wire on said mounting board. 2. A multi-chip module according to claim 1, Suzuki et al. show wherein said plurality of first semiconductor chips include a microcomputer, a RAM and a signal processing device for processing signals for specific applications, respectively and wherein said second semiconductor chip is a nonvolatile memory.

3. A multi-chip module according to claim 2, Taguchi show wherein said microcomputer and said RAM or said signal processing device for processing the signal for specified application which is connected to said microcomputer are interconnected by wiring formed on the mounting board by imposition; and wherein said microcomputer includes

an exclusive interface corresponding to said nonvolatile memory, said microcomputer and said nonvolatile memory being interconnected through said bonding wire.

4. A multi-chip module according to claim 3, Taguchi show wherein said nonvolatile memory is mounted back-to-back with said first semiconductor chips including said microcomputer.

5. A multi-chip module according to claim 4, Taguchi show wherein said first semiconductor chips mounted back-to-back with said nonvolatile memory include said microcomputer and said RAM; and wherein the long side of the semiconductor chip constituting said RAM and the long side of the semiconductor chip constituting said nonvolatile memory are arranged orthogonally to each other.

[0026] FIG. 1A and FIG. 1B are a cross sectional view and a perspective view showing a hybrid integrated circuit in accordance with an embodiment of the present invention. In this case, the hybrid integrated circuit 1 is composed of a ceramic substrate or a printed circuit board 3 as a common substrate in which are formed electrode patterns such as electrode pads for bonding, wiring patterns and so forth, a monolithic semiconductor integrated circuit 5 of an ASIC mounted on the ceramic substrate 3, another monolithic semiconductor integrated circuit 7 of an FPGA also mounted on the ceramic substrate 3 and gold wires 9 with which the monolithic semiconductor integrated circuits 5 and 7 and the ceramic substrate 3 are interconnected. These monolithic semiconductor integrated circuits 5 and 7 have been diced as semiconductor chips from a semiconductor wafer.

[0027] The monolithic semiconductor integrated circuit 5 and the monolithic semiconductor integrated circuit 7 are designed to cooperate with each other by exchanging signals through the electrode pads and the wiring patterns on the common substrate in order to implement prescribed functions. After mounting these monolithic semiconductor integrated circuits 5 and 7 on the ceramic substrate 3 and making necessary electric connection therebetween and with the electrode pads to which external leads are connected, they are sealed with an insulating material such as, e.g., an expoxy regin, in the form of multi-chip-package as an individual semiconductor integrated circuit product which provides particular functions for a specific purpose.

[0050] For example, while the ASIC 5 and the FPGA 7 are mounted side by side on the ceramic substrate 3 in the case of the hybrid integrated circuit in accordance with the present invention as illustrated in FIG. 1A and FIG. 1B, it is also possible to mount the ASIC 5 on the ceramic substrate 3 and then mount the FPGA 7 on the ASIC 5 as illustrated in FIG. 1C with a group of solder or gold balls for electrical connection therebetween. Inversely, it is possible to mount the FPGA 7 on the ceramic substrate 3 and then mount the ASIC 5 on the ASIC 5 with a group of solder or gold balls for electrical connection therebetween. This is called a stack type of the hybrid integrated circuit. Also, the external terminals of the hybrid integrated circuit may be designed not only as QFP (Quad Flat Packege) as illustrated in FIG. 1A but also as BGA (the ball grid array) as illustrated in FIG. 8. In this case, the electrodes provided at the bottom surface of the hybrid integrated circuit function as the external terminals.

[0052] As detailedly explained in the above, in accordance with the hybrid integrated circuit of the present invention, it is possible to make effective use of both the characteristics of an ASIC and the characteristics of an FPGA. Namely, it is possible to provide a hybrid integrated circuit whose specification can quickly be modified and adjusted without need for preparing a new mask and without need for compromising the performance of the hybrid integrated circuit. Namely, there are many advantages, i.e., the reduction of production cost and the flexibility (programmablility) responsible to the change of the specification of the system. Also, when the hybrid integrated circuit is implemented with a general purpose flash-type FPGA, a surplus area of the flush memory of the FPGA is used as a non-volatile storage for operation of the ASIC of the hybrid integrated circuit. Furthermore, when the hybrid integrated circuit is implemented with a general purpose SRAM-type FPGA, a surplus area of the SRAM of the FPGA is used as a temporary storage for operation of the ASIC of the hybrid integrated circuit. Accordingly, it is possible to reduce the cost and minimize the size of the hybrid integrated circuit and the amount of real estate or area it occupies on the circuit board.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/686,685,723,777,728,724,725,e25.011,e23.173,e25.012,e25.023,e23.149,e23.055,e23.069,e23.023	6/8/06
Other Documentation: foreign patents and literature in 257/686,685,723,777,728,724,725,e25.011,e23.173,e25.012,e25.023,e23.149,e23.055,e23.069,e23.023	6/8/06
Electronic data base(s): U.S. Patents EAST	6/8/06

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
6/8/06